Challenges for the upscaling of the Tandem Si / PK technology

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The crystalline Silicon (c-Si) / Perovskite (PK) 2 terminal (2T) Tandem solar cells have recently reached a certified power conversion efficiency (PCE) of 33.7% [1], exceeding the theoretical limit of silicon single junction. This makes this tandem a good growth driver for the PV technology. Those results are really promising but are still obtained at lab scale on small size devices (≤1cm²), the perovskite technology being less mature than the well-established Silicon one. In order to reduce time to market of this new technology, several challenges remain in order to upscale the materials and the processes toward the industry.
The objective of the presented work is to develop efficient Perovskite/Silicon tandem devices that can be manufactured with techniques compatible with the next generation PV industry. Starting from 8.45 cm² devices with PIN architectures, with PCE above 27 %, CEA is developing materials and processes compatible with industrial requirements. Several bottlenecks are identified and will be discussed.

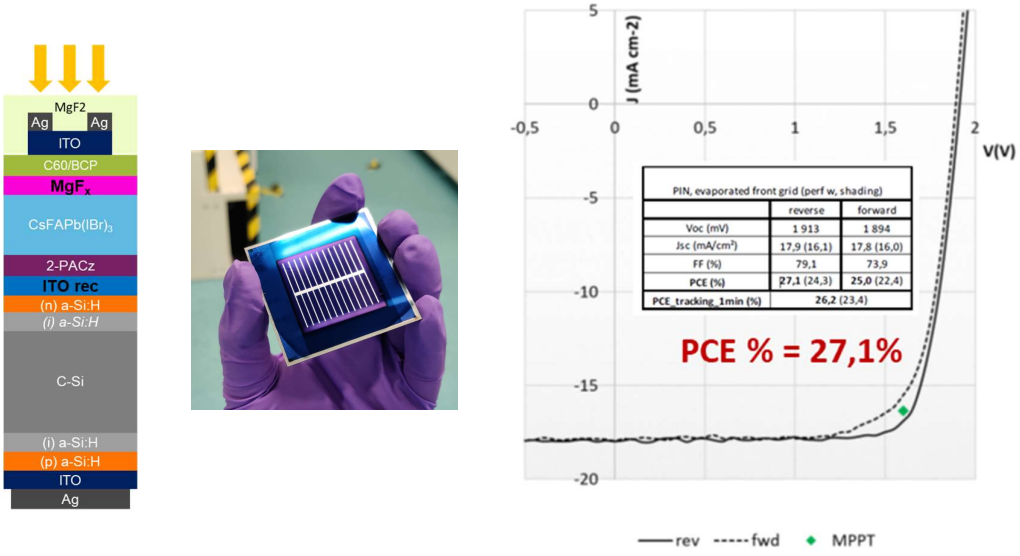

Figure 1: Left) PIN architectures developed at INES; Middle) Picture of 8.45 cm² active area cell on the 5x5 cm² substrate. Right) JV curves of a tandem device in reverse scan (full line) and forward scan (dashed lines). The green diamond indicates the Maximum Power Point Tracking.

References

[1] https://www.kaust.edu.sa/en/news/kaust-team-sets-world-record-for-tandem-solar-cell-efficiency; https://www.perovskite-info.com/kaust-team-announces-337-efficiency-perovskitesilicon-tandem-solar-cell