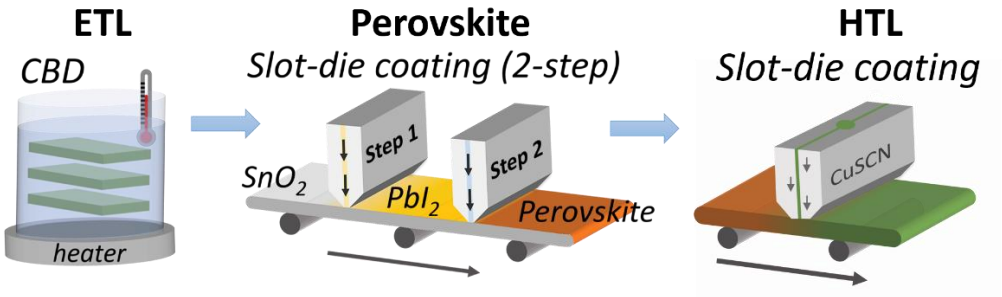
Strategies in scale-up of perovskite solar cells: From small laboratory cells to modules

Iwan Zimmermann[1], Thomas Guillemot[1], Marion Provost[1], Salim Mejaouri[2], Celia Aider[2], Van Son Nguyen[1], K. M. Muhammed Salim[1], Alexandre Blaizot[1], Nao Harada[1], Daniel Ory[2], Stefania Cacovich[3], Jean Rousset[2]

[1] *Institut Photovoltaïque d'Île-de-France (IPVF), Palaiseau, 91120, France.*
[2] *Électricité de France (EDF) R&D, Palaiseau, 91120, France.*
[3] *CNRS, École Polytechnique, IPVF, UMR 9006, Palaiseau, 91120, France.*
iwan.zimmermann@ipvf.fr

Single junction perovskite solar cells (PSC) already achieved certified power conversion efficiencies beyond 26%, which is comparable to state-of-the-art monocrystalline silicon solar cells. However, these results are realized on very small active areas - typically in the range of 0.1 cm^2. Reported efficiencies on larger areas are generally much lower than compared with the small devices. The record for a perovskite module on the NREL chart currently stands at 18.6% for 800 cm^2.[1] This drop in efficiency on one hand can be explained due to the modularization. P1-P2-P3 laser patterning is commonly applied to connect perovskite sub cells in series to avoid resistive losses from the transparent conductive oxides. On the other hand, the uniform deposition of the different thin films in a PSC on the large scale is challenging. While spin-coating is generally used in fabricating highly efficient small devices this technique has its limitations in terms of scale-up. Our work focuses on the quest of optimizing industrially compatible wet deposition techniques for the entire PSC stack in a NIP configuration. The use of materials with proven long-term stability and low cost thereby plays an important role in view of future commercialization of the PSC technology. Chemical bath deposition (CBD) is used to deposit tin oxide that acts as the electron extracting layer. We investigated the deposition mechanism and optimum number of CBD cycles to achieve the best performance and reproducibility.[2] Perovskite films are grown by sequential slot-die coating.[3] This 2-step deposition method allowed us to deposit perovskite films up to 10 x 10 cm^2. Finally, for the hole extraction layer, CuSCN is deposited onto the perovskite film using slot-die coating. We systematically optimize ink composition and slot-die parameters to achieve desired film thickness and uniformity. Results on small devices as well as on mini-modules for the fully up-scalable device architecture are presented.



References

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